VGA CMOS Image Sensor

BF3A03

Datasheet

1. General Description

The BF3A03 is a highly integrated VGA camera chip which includes CMOS image sensor (CIS) and image signal processing function (ISP). It is fabricated with the world's most advanced CMOS image sensor process to realize ultra-low dark noise, high sensitivity and very low power imaging system. The sensor consists of a 648 x 488 effective pixel array which has an optical format of 1/6.5 inch. It has integrated noise canceling CDS (Correlated Double Sampling) circuits, analog global gain and separated R/G/B gain controller, auto black level compensation and on-chip 10-bit ADC. The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB444, RGB555, RGB565, YCBCR 4:2:2. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

The product is capable of operating at up to 60 frames per second at 48MHZ clock in VGA mode, with complete user control over image quality and data formatting. All required image processing functions, including exposure control, white balance control, color saturation control and so on, are also programmable through the two-wire serial bus.

2. Features

- Standard optical format of 1/6.5 inch.
- 30 frame/sec VGA mode @ 24MHz master clock.
- 60 frame/sec VGA mode @ 48MHz master clock.
- Ultra-low dark noise at high temperature.
- Various output formats: YCBCR4:2:2, RGB444, RGB555, RGB565, Raw Bayer (648 x 488).
- Power supply: 2.7~3.1V for core, 1.7~3.1V for I/O.
- Horizontal /Vertical mirror.
- 50/60Hz flicker cancellation.
- Programmable I/O drive capability.
- Automatic black level control.
- Image processing function: Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, Skin Detection, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation and Contrast, and Data Format Conversion.
- On-chip test pattern generation of many types including customer programmable
- Package: CSP, Bare Die

3. Applications

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

4. Technical Specifications

- Active pixel array: 648 x 488
- Pixel size: 3.15μm×3.15μm
- Sensitivity: 2.5V/lux.s
- Dark current: 1 mV/S at 40℃
- Power consumption: TBD
- Standby current: 30uA
- S/N Ratio: 42dB
- Dynamic range: 58dB
- Operating temperature: -20~60℃
- Stable Image temperature 0~50℃
- Optimal lens chief ray angle: 27º

5. Functional Overview

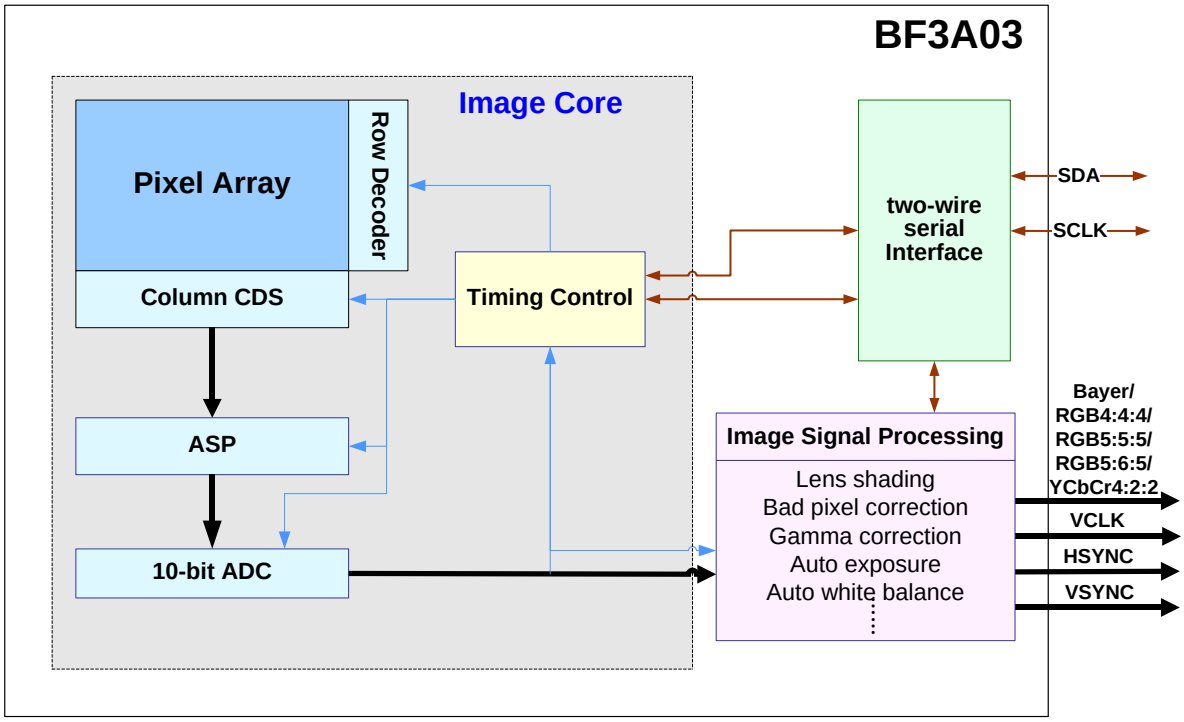


Figure 1. Block Diagram

BF3A03 has an active image array of 648x488 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The ASP block is mainly used to control global gain and color gains to get accurate exposure and white balance under different light condition and color temperature. The analog signal is transferred to digital signal by A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, low pass filter, color correction, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

5.1 Pixel Array

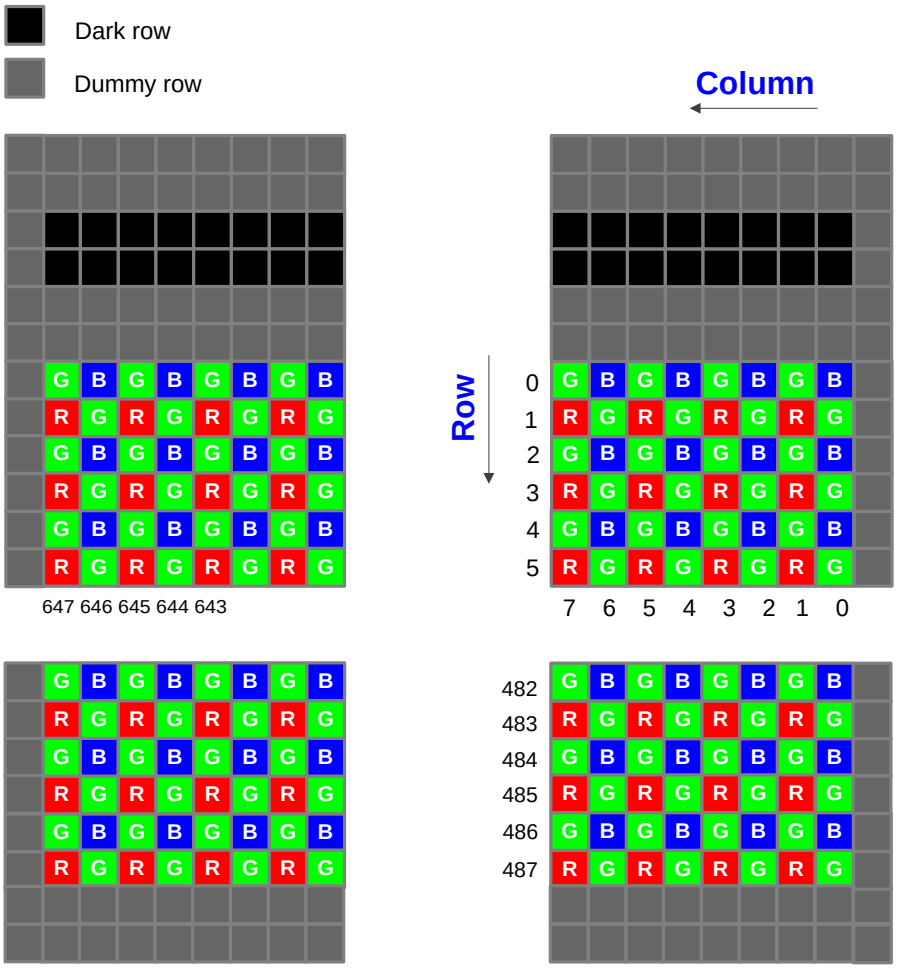


Figure 2. Sensor Array Region

The active pixel array is configured as 648 columns by 488 rows. Dummy pixels and dark rows are added outside the active pixel array.

Pixel array is covered by Bayer color filters as can be seen in the figure2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel. BF3A03 can provide the Raw Bayer data or YUV data through an 8-bit output data bus. If no flip in column, column is read out from 0 to 647. If flip in column, column is read out from 647 to 0. If no flip in row, row is read out from 0 to 487. If flip in row, row is read out from 487 to 0. In this way, the output pixel color order is different with row flip and column flip.

5.2 Column CDS

BF3A03 has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented

column buffer amplifier and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Timing controller

The timing controller controls the following functions

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- External timing outputs (VSYNC, HREF and VCLK)

5.4 Analog Signal Processor

This block performs all analog image functions including Color gain/Global gain control and black level compensation. Each of the R, G, B color pixel signals can be multiplied by different gain factors to balance the color of the image at various light conditions.

5.5 A/D converter

The analog signals are converted to digital forms column by column and row by row, throughout the whole array. BF3A03 provides the 10-bit Raw Bayer data for ISP through an internal 10-bit data bus.

5.6 Automatic Black Control

The automatic black level controller calculates the data of the dark row and controls the lowest black level for output image data.

5.7 Image Signal Processor

This block performs all image processing functions including Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Skin detection, Auto exposure, Auto White Balance, Color Saturation, Contrast, and Data Format Conversion.

6. Specifications

6.1 Electrical Characteristics

6.1.1. Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.1 V
- Supply voltage (VDD3A): 2.7 ~ 3.1 V
- Operating temperature: -20~60 ℃
- Storage temperature: -30~80 ℃
- ESD Rating, Human Body mode: 2000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2. DC Parameters

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	2.8	3.1	
VDD3A	Analog power supply	V	2.7	2.8	3.1	--
I_vddio	VDDIO supply current, normal operation mode	mA	--	15.0	--	1
I_vdd3a	VDD3A supply current, normal operation mode	mA	--	10.0	--	2
Vih	Input voltage logic “1”	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic “0”	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic “1”	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic “0”	V	--	--	0.1*VDDIO	--

Table 1. DC Operation Conditions

Note：

1. Power consumption of I/O depends on the output load and system environment, user should supply enough current to sensor for stable operation.
2. The current of analog circuit depends on the registers’ values; it is measured at specific register’s value.

6.1.3. Clock Requirement

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External clock frequency	MHz	6	24	--	1

MCLK	Master clock	MHz	--	24	48	2
PCLK	Pixel clock	MHz	--	12	24	3
VCLK	Output clock	MHz	--	24	48	4
SCLK	two-wire serial interface clock frequency	KHz	--	400	--	5
Inormal	Current in YUV4:2:2 output mode	mA	--	25	35	6
Idown	Current in power down mode	uA	--	30	--	7

Table 2. AC Operation Conditions

Note:

1. XCLK is the input clock and it is the input of PLL.
2. MCLK is the master clock of the system, and it can be generated by PLL.
3. PCLK is the pixel clock and its frequency is half of MCLK's.
4. VCLK is the output clock of the system.
5. SCLK is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section
6. VDDIO=2.8V, VDD3A=2.8V (YUV4:2:2 output).
7. Hardware power down.

6.2 Electro-Optical Characteristics

Clock frequency: 24MHz.

Operating voltage: VDDIO=2.8V, VDD3A=2.8V.

Operating temperature: 25°C

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	2.5		1
Dark current	mV/sec	--	1	3	2
S/N ratio	dB	--	42dB	--	--
Dynamic Range	dB	--	58dB	--	--
Frame Rate	fps	--	30	60	3

Table 3. Electro-Optical Characteristics

Notes:

1. With color filter, measured at 50 lux green light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (40 Celsius).
3. Max frame rate with 648×488 window size at MCLK 48MHz.

6.3 Input-Output AC Characteristics

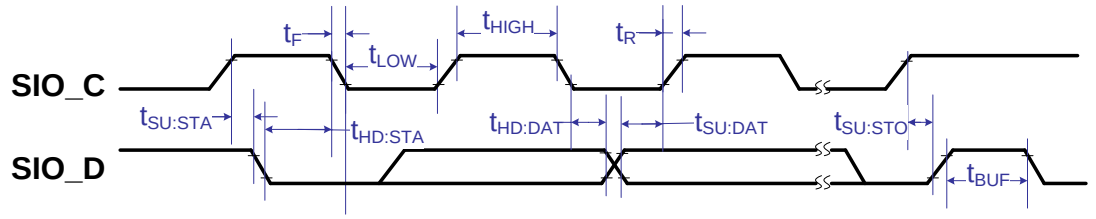


Figure 3. Two-Wire Serial Interface Timing

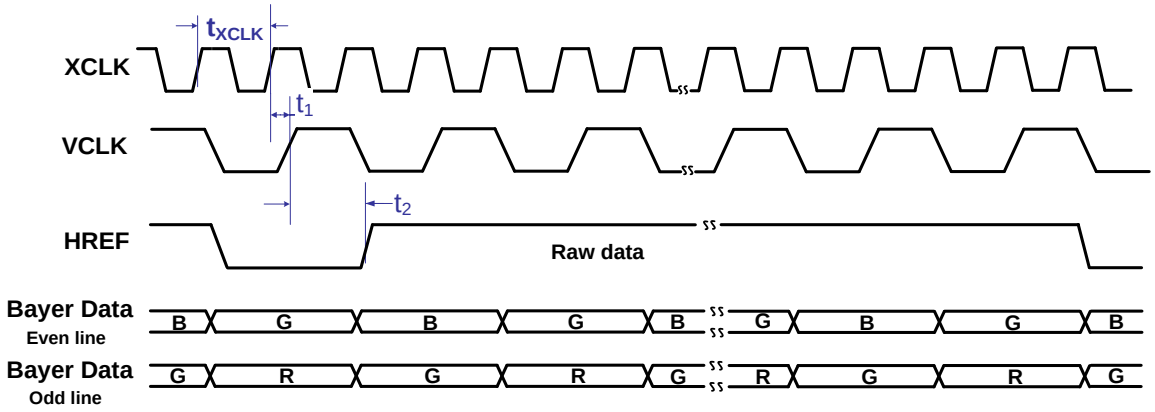


Figure 4. Horizontal Timing Raw Bayer Data

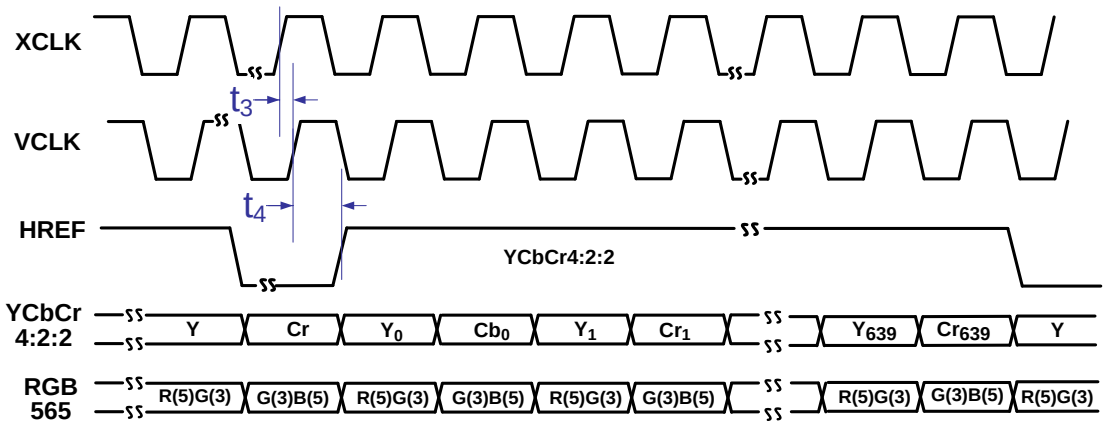


Figure 5. Horizontal Timing YUV4:2:2

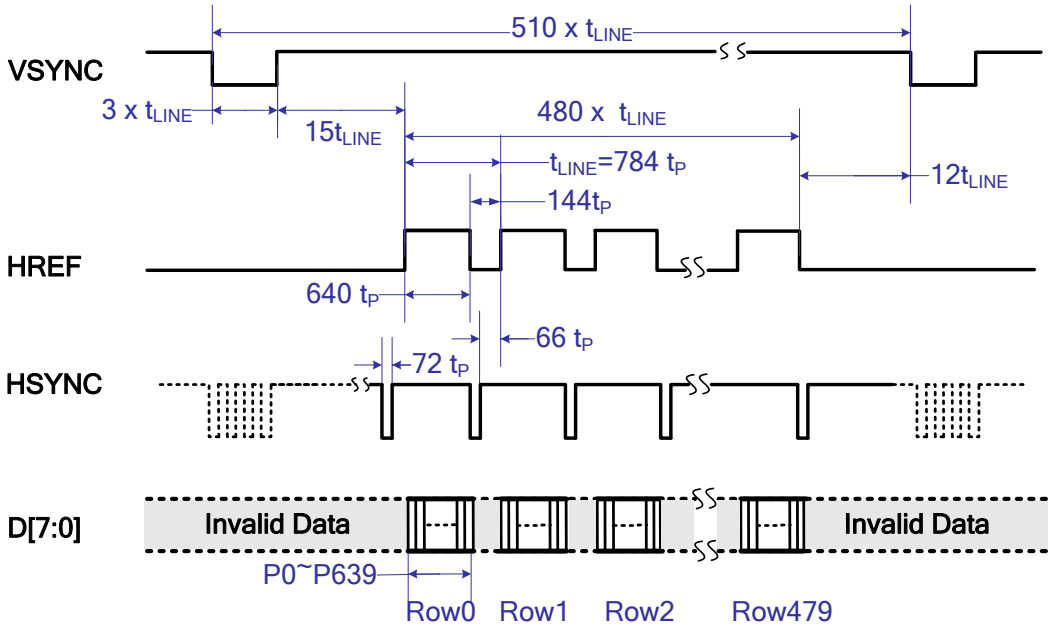


Figure 6. VGA Frame Timing

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	t_P=2 x t_{MCLK}	41.6	83.2	--	ns
f_{MCLK}	Master Clock Frequency	--	24	48	MHz
f_{VCLK}	Video Clock Frequency for Raw data , f_V= f_{MCLK} /2 for YUV/RGB , f_V= f_{MCLK}	--	24	48	MHz
t_{LINE}	Line length	--	784x t_P	--	ns
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns
t1	XCLK rising to VCLK (RAW DATA)	--	28.8	--	ns
t2	VCLK rising to HREF (RAW DATA)	--	43.8	--	ns
t3	XCLK rising to VCLK (YUV)	--	19.2	--	ns
t4	VCLK rising to HREF (YUV)	--	21.6	--	ns

Table 4. AC Characteristics

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

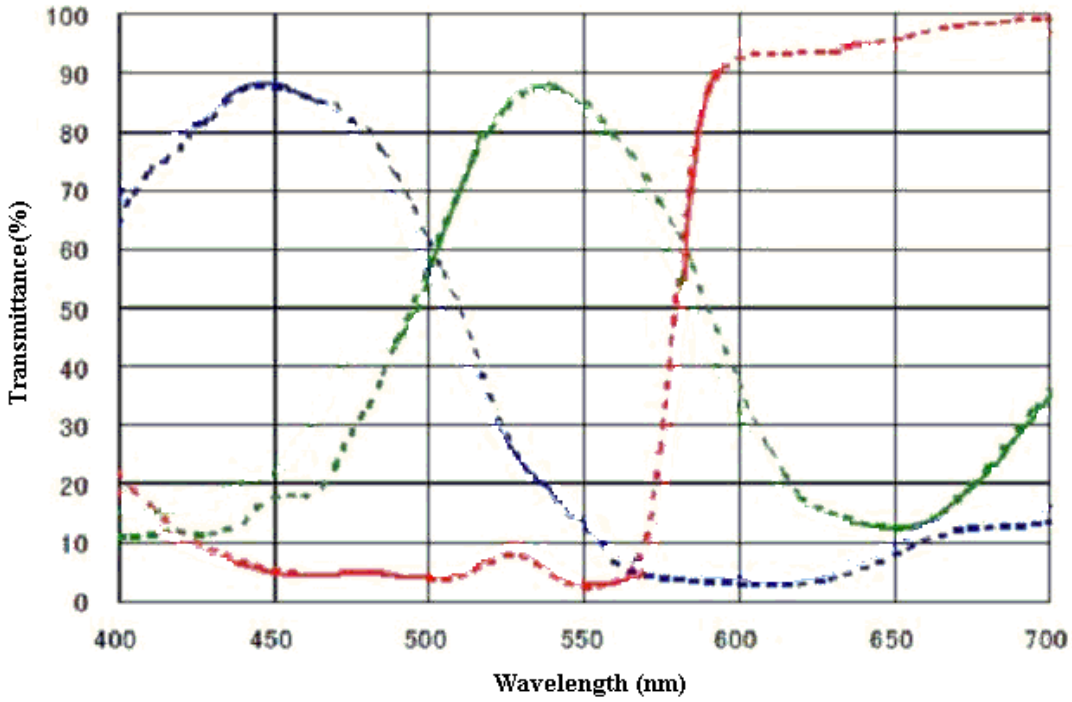


Figure 7. Spectral Characteristics

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF3A03 are written and read through the two-wire serial interface. BF3A03 has two-wire serial interface slave. BF3A03 is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out of BF3A03 through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 4.7kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF3A03 is 6eh.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A “0” in the LSB of the address indicates write mode, and “1” indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device’s 8-bit address. The last bit of the address determines if the request will be a read or a write, where “0” indicates write and “1” indicates read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF3A03 uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

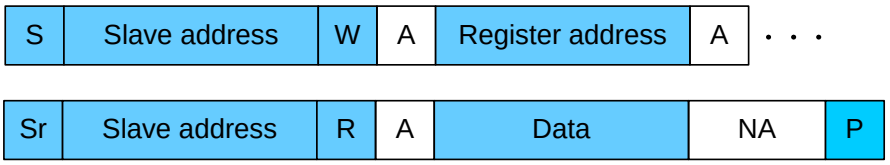
A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

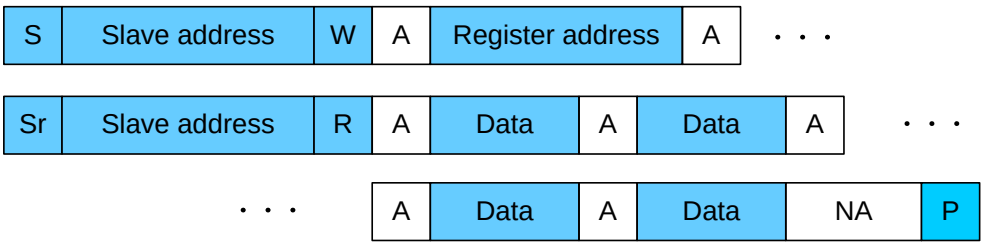
Single Write Mode Operation

Multiple Write Mode (Register address is increased automatically) [1] operation

Single Read Mode Operation



Multiple Read Mode (Register address is increased automatically) [1] Operation




From master to slave


From slave to master

S: Start condition. **Sr:** Repeated Start (Start without preceding stop.)

Slave Address: write address = DCh = 11011100b

read address = DDh = 11011101b

R/W: Read/Write selection. High = read, LOW = write.

A: Acknowledge bit. **NA:** No Acknowledge.

Data: 8-bit data **P:** Stop condition

Note: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 Register Summary (full list)

Address	Name	Width	Default value	Description
00h	***DBLKEB_I2C/DBLKEG_I2C***	6	22h	Bit[7:6]: reserved Bit[5:0]: Coarse positive offset adjust for even col (manual), when I2C_SWITCH(0X61[6])==1'b1,write or read DBLKEB; when I2C_SWITCH(0X61[6])==1'b0,write or read DBLKEG.
01h	***BLUE_GAIN***	6	19h	Blue gain register.
02h	***RED_GAIN***	6	15h	Red gain register.
03h	***VHREF***	8	00h	VREF and HREF Control, Bit[7:6]: VREF end low 2 bits(high 8 bits at VSTOP[7:0]), Bit[5:4]: VREF start low 2 bits (high 8 bits at VSTART[7:0]), Bit[3:2]: HREF end low 2 bits (high 8 bit at HSTOP[7:0]), Bit[1:0]: HREF start low 2 bits (high 8 bits at HSTART[7:0]).
04h	***DARKEB_AVER /DARKEG_AVER***	8	10h	Bit[7:0]: Reserved
05h	***DARKOG_AVER /DARKOR_AVER***	8	10h	Bit[7:0]: Reserved
06h	***DBLK_CNTL1***	8	78h	Bit[7:0]: Reserved
07h	***DBLK_AJ_STEP***	8	49h	Bit[7:0]: Reserved
08h	***TAREG3***	8	00h	Bit[7:0]: Reserved
09h	***COM2***	8	d5h	Bit[7]: Standby mode, 0: Disable standby mode, 1: Enable standby mode. Bit[6]: SDA output drive capability control 0: 4mA; 1: 8mA(default); When TDREG[6]=1 Bit[5:4]:VCLK output drive capability 00: 4mA 01: 8mA 10: 12mA 11: 16mA Bit[3:2]: HSYNC output drive capability 00: 4mA 01: 8mA 10: 12mA 11: 16mA Bit[1:0]: Data output drive capability 00: 4mA 01: 8mA 10: 12mA 11: 16mA When TDREG[6]=0 Bit[1:0]: Data & VCLK & HSYNC output drive capability 00: 4mA 01: 8mA 10: 12mA 11: 16mA
0ah	***COM5***	8	21h	Common Control 5, Bit[7:4]: Total columns number(M1) for CK-GATE subsample; Bit[3:0]: Columns selected number(M2) for CK-GATE subsample. Note: Set M3 (set by register COM8[3:0]) columns to a package, and select M2 columns from M1 columns.
0bh	***COM4***	8	00h	Common Control 4, Bit[7]: Row Selected in CK-GATE Mode, 0: Select even row, 1: Select odd row; Bit[6]: Column Selected in CK-GATE Mode, 0: Select even column, 1: Select odd column. Bit[5]: 0: Output normal HSYNC/VSYNC; 1: Output fixed value: HSYNC=HSYNC_VAL, VSYNC=VSYNC_VAL Bit[4]: Fixed Value of Output VSYNC, If SYNC_MODE=1&SYNC_VALU=0,output VSYNC=0/HSYNC=0; If SYNC_MODE=1&SYNC_VALU=1, output VSYNC/HSYNC=1; Else, VSYNC/HSYNC=normal; Bit[3:0]: Skip frame count.
0ch	COM3	8	00h	Common Control 3, Bit[7]: Processed Raw Data Control, 0: Processed raw data from YCBCR to RGB conversion in DATFORMAT module, 1: Processed raw data from color interpolation (Processed by Lens Shading Correction, Gamma Correction, Bad Pixel Correction, Cluster Correction, and De-noise); Bit[6]:Output data MSB and LSB swap

				Bit[5:4]: Output Processed Raw Data Sequence (When 0x0c[7]=0), 00: (LINE0: BGBG/LINE1: GRGR), 01: (LINE0: GBGB/LINE1: RGRG), 10: (LINE0: GRGR/LINE1: BGBG), 11: (LINE0: RGRG/LINE1: GBGB); Bit[3]:0:No HREF when VSYNC_DAT=0; 1:Always has HREF no matter VSYNC_DAT=0 or not; Bit[2]: 0: Normal, 1: DATA is ahead one MCLK(YUV) or PCLK (Raw data) of HREF/CKSUB; Bit[1]: 0: Normal, 1: HREF is ahead one MCLK(YUV) or PCLK (Raw data) of DATA; Bit[0]: 0: Normal, 1: HREF is ahead 0.5 MCLK(YUV) or PCLK (Raw data) of DATA
0dh	***DBLKOG_I2C/DBLKOR_I2C***	6	22h	Bit[7:6]: Reserved Bit[5:0]: Coarse positive offset adjust for odd col(manual), When I2C_SWITCH(0X61[6])==1'b1,write or read DBLKOG; When I2C_SWITCH(0X61[6])==1'b0,write or read DBLKOR.
0eh	***DBLK_TAR_EG***	8	20h	Black control target for odd line even col(EG)
0fh	***AVER_OR***	8	ROh	Read out black aver for OR, this value is only adjusted by analog adjustment
10h	***COM6***	8	21h	Common Control 6, Bit[7:4]: Total rows number (N2) for gate subsample; Bit[3:0]: Rows selected number (N1) for gate subsample. Note: Set N3 rows (Set by register COM8 [7:4]) to a package, and select N1 rows from N2 rows.
11h	***CLKRC***	8	10h	Bit[7]:MCLK_ISP1 inverse 0: reverse, 1: no reverse. Bit[6:5]: MCLK_ISP1 delay select 00: delay 0ns, 01: delay 2ns, 10: delay 4ns, 11: delay 7ns. Bit[4]:MCLK_ISP2 inverse 0: reverse, 1: no reverse. Bit[3:2]: MCLK_ISP2 delay select 00: delay 0ns, 01: delay 2ns, 10: delay 4ns, 11: delay 7ns. Bit[1:0]: MCLK_SEL1 00: Divide by 1, 01: Divide by 2, 10: Divide by 4, 11: no clock.
12h	***COM7***	8	00h	Common Control 7, Bit[7]: SCCB Register Reset, 0: No change, 1: Resets all registers to default values. Bit[6]: Reserved; Bit[5]: Row 1/2 Subsample Selection, 0: Enable 1/2 subsample (When 0x4a[2] and 0x4a[0] is 1'b1), 1: Normal; Bit[4]: 1/2 Digital Subsample Selection (Only for YUV422/RGB565/RGB555/RGB444 output), 0: VGA, 1: QVGA; Bit[3]: Reserved; Bit[2]: YUV422/RGB565/RGB555/RGB444 Selection; Bit[1]: Reserved; Bit[0]: Raw RGB Selection, {0x12[2],0x12[0]} 00: YUV422, 01: Raw Data, 10: RGB565/RGB555/RGB444 (Used with 0x3a), 11: Processed Raw Data (Used with 0x0c[7]).

13h	***COM8***	8	07h	Bit[7]: 1:AE_TAR 0:AE_TAR_MODIFY (decrease the target brightness based on the number of over exposure pixels) Bit[6]: 0: Digit gain disable; 1:Digit gain enable Bit[5]: The high Bit of INT_STEP_60 Bit[4]: The high Bit of INT_STEP_50. Bit[3]: GLB_GAIN0 written is effective when AGC disable 0:GLB_GAIN0 written disable 1:GLB_GAIN0 written enable Bit[2]: AGC Enable. 0: Disable 1: Enable Bit[1]: AWB Enable. 0:Disable , 1: Enable. Bit[0]: AEC Enable. 0:Disable , 1: Enable.
14h	***P_PIXEL_OE***	8	read only	The number of the over exposure pixels used to modify the target brightness and the adjusting speed.
15h	***COM10***	8	02h	Common Control 10, Bit[7]: VCLK before CK-Gate reverse; Bit[6]: 0: HREF, 1: HSYNC; Bit[5]: 0: Output VSYNC_IMAGE, 1: Output VSYNC_DAT; Bit[4]: VCLK after CK-Gate reverse ; Bit[3]: HREF Mode, 0: No HREF when VSYNC_DAT=0, 1: Always has HREF no matter VSYNC_DAT=0 or not; Bit[2]: Reserved; Bit[1]: VSYNC Option, 0: Active low, 1: Active high; Bit[0]: HSYNC Option, 0: Active high, 1: Active low.
16h	***BIAS2***	8	22h	Bit[7]:Reserved Bit[6:4]: IBIAS for black step 000:1uA,4mV (4mV*1024/800mV=5LSB); 001:1.5uA,6mV(6mV*1024/800mV=7.5LSB) 010: 2uA,8mV (8mV*1024/800mV=10LSB); 011:2.5uA,10mV(10mV*1024/800mV=12.5LSB) 100:3uA,12mV (12mV*1024/800mV=15LSB); 101:3.5uA,14mV(14mV*1024/800mV=17.5LSB); 110:4uA,16mV (16mV*1024/800mV=20LSB); 111:4.5uA,18mV(18mV*1024/800mV=22.5LSB) Bit[3:0]: Control the bias current of pixel: 0000:10uA 0001:20uA 0010:25uA 0011:35uA 0100:30uA 0101:40uA 0110:45uA 0111:50uA 1000:50uA 1001:60uA 1010:65uA 1011:75uA 1100:70uA 1101:80uA 1110:85uA 1111:95uA
17h	***HSTART***	8	00h	Output Format-Horizontal Frame (HREF column) start high 8-bits (low 2 bits at HREF[1:0]).
18h	***HSTOP***	8	a0h	Output Format-Horizontal Frame (HREF column) end high 8-bits (low 2 bits at HREF [3:2]).
19h	***VSTART***	8	00h	Output Format-Vertical Frame (row) start high 8-bits (low 2 bits at VREF [5:4]).
1ah	***VSTOP***	8	78h	Output Format-Vertical Frame (row) end high 8-bits (low 2 bits at VREF [7:6]).
1bh	***PLLCTL***	8	09h	PLL_OUT=2*Fin*y/xz (default=2*24MHz*4/(4*1)=48MHz) Bit[7]: PLL feedback divider(y) 0:Divided by 4(y=4) 1:Divided by 3(y=3) Bit[6]: PLL output divider(z): 0:Divided by 1(z=1) 1:Divided by 2(z=2) Bit[5:4]: PLL input divider(x): 00:divided by 1(x=1) 01:Divided by 2(x=2) 1x:Divided by 4(x=4) Bit[3]: PLL control 0: Enable PLL, 1: Disable PLL, default; Bit[2]:XCLK select 0:Use XCLK directly from input pad; 1:Use XCLK after deglitch Bit[1]: Reserved

				Bit[0]: VCLK_OUT_EN 0: No VCLK 1:Normal VCLK
1ch	***MIDH***	8	7fh,RO	Manufacturer ID MSB
1dh	***MIDL***	8	a2h,RO	Manufacturer ID LSB
1eh	***GLB_GAIN_CNTL MACULA_AUTO_EN MVFP***	8	40h	Mirror/Vertical Flip Control, Bit[7]: 0: GLB_GAIN delay a frame, 1: GLB_GAIN no delay; Bit[6]: The Black Sun Control, 0: Disable black sun, 1: Enable black sun; Bit[5]: Mirror, 0: Normal image, 1: Mirror image; Bit[4]: Vertical Flip, 0: Normal image, 1: Vertically flip image; Bit[3:0]: Reserved.
1fh	***DBLK_TAR_EB***	8	20h	Black control target for even line even col(EB)
20h	***TDREG***	8	24h	Bit[7]: DR_EXTR 0:no extral HSYNC/VCLK drive capability 1:extral HSYNC/VCLK drive capability:4mA Bit[6]: DR_SEL:output PAD drive capability select Bit[5:3]: ISEL_E[2:0],select level of black level's negative terminal for even channel: 000: 32mV 001:64mV 010:96mV 011:128mV 100:164mV 101:196mV 110:224mV 111:256mV Bit[2:0]: ISEL_O[2:0],select level of black level's negative terminal for odd channel: 000: 32mV 001:64mV 010:96mV 011:128mV 100:164mV 101:196mV 110:224mV 111:256mV
21h	***TAREG***	8	70h	Bit[7]:Reserve Bit[6]: VDDP power control 0: Normal(VDDP=VDD3A); 1: VDDP power on; bit[5:4]: Output VDDP select: 00:2.3V, 01:2.4V, 10:2.5V, 11:2.6V Bit[3]:Reserve Bit[2]:Output VCLK[9:0] pad tri state: 1:Tri state, 0:No tri state Bit[1]:Output SYNC[9:0] pad tri state: 1:Tri state, 0:No tri state Bit[0]:Output DATA[9:0] pad tri state: 1:Tri state, 0:No tri state
22h	***DBLK_TAR_OG***	8	20h	Black control target for even line odd col(OG)
23h	***GLGAINREG***	7	33h	Green Gain[2:0], Bit[6:4]: G1 Gain (Used as Green gain [2:0] of even column), Bit[2:0]: G2 Gain (Used as Green gain[2:0] of odd column).
24h	***AE_TAR1***	8	4fh	Bit[7]: 0:The macula estimate is relate to bright . 1:The macula estimate is not relate to bright . Bit[6:0] :Y target value. Actually,{0x24[6:0],1'b0} is used.
25h	***AE_LOC***	8	88h	Bit[7:4]: INT_TIME lock Bit[3:0]: Global Gain lock
26h	***DBLK_TAR_OR***	8	20h	Black control target for odd line odd col(OR)
27h	***DBLK_LOCK***	8	96h	Bit[7:0]: Reserved
28h	***DBLK_CNTL0***	8	ffh	Fine(digital) and Coarse positive(analog)offset adjust control: Bit[7]:Digital offset adjust for EB: 1:Auto; 0:Manual; Bit[6]:Digital offset adjust for OG: 1: Auto; 0:Manual; Bit[5]:Digital offset adjust for EG: 1: Auto; 0:Manual; Bit[4]:Digital offset adjust for OR: 1:Auto; 0:Manual; Bit[3]:DBLKEB 1:Auto; 0: Manual; Bit[2]:DBLKOG 1:Auto; 0: Manual; Bit[1]:DBLKEG 1:Auto; 0: Manual; Bit[0]:DBLKOR 1:Auto; 0: Manual.

29h	***BIAS1***	8	20h	Bit[7]:Reserve Bit[6:5]: Gen_ref of ADC:(mid/pref/nref): 00:mid=1.3640v pref=1.7537v nref=0.9743v 01:mid=1.4001v pref=1.8001v nref=1.0000v 10:mid=1.4312v pref=1.8401v nref=1.0222v 11:mid=1.5272v pref=1.9635v nref=1.0908v Bit[4:2]: BSWITCH,control bias of ADC:(input_ibias=10ua), 000:10uA, 001:15uA, 010:20uA 011:25uA, 100:30uA, 101:35uA, 110:40uA, 111:45uA, Bit[1:0]:Control the bias current of asp: 00:5uA 01:10uA 10: 15uA(default) 11:20uA
2ah	***EXHCH***	8	00h	Dummy Pixel Inserted MSB, Bit[7:4]: Dummy pixel inserted in horizontal direction 4 MSB; Bit[3:0]: Reserved.
2bh	***EXHCL***	8	00h	Dummy Pixel Inserted LSB, Dummy pixel inserted in horizontal direction 8 LSB.
2ch	***AVER_EB***	8	RO	Read out black aver for EB,this value is only adjusted by analog adjustment
2dh	***AVER_EG***	8	RO	Read out black aver for EG,this value is only adjusted by analog adjustment
2eh	***AVER_OG***	8	RO	Read out black aver for OG,this value is only adjusted by analog adjustment
2fh	***DREF***	8	42h	Bit[7:2]: Reserved Bit[1]: System CLK select: 1:XCLK 0:PLL_CLK
30h	***HSYST***	8	60h	Control the rising edge of HSYNC,HSYNC rising edge low 8 Bits
31h	***HSYEN***	8	14h	Control the falling edge of HSYNC,HSYNC falling edge low 8 Bits
33h	***OFFSET***	8	RO	Auto offset for lens shading correction (same as black_aver).
34h	***OFFSET_REG***	8	1dh	Manual written offset for lens shading correction.
35h	***R_COEF***	8	46h	Lens shading correction gain for R pixel.
36h	***OFFSET_MODE*** ***GAIN_SEL*** ***y0h_g*** ***y0h_b*** ***x0h_g*** ***x0h_b***	8	45h	Bit[7]: OFFSET_MODE, 0: Using auto offset for lens shading correction, 1: Using manual written offset for lens shading correction. Bit[5]:The vertical center high 1 bit of G. (vertical center); Bit[4]: The vertical center high 1 bit of B.(vertical center); Bit[3:2]: The horizontal center high 2 bits of G (horizontal center); Bit[1:0]: The horizontal center high 2 bits of B. (horizontal center).
37h	***y0l_b***	8	f4h	The vertical center low 8 bits of B (vertical center).
38h	***x0l_b***	8	44h	The horizontal center low 8 bits of B (horizontal center).
39h	***MAN_OFFSET*** ***OFFSET_ME***	8	a0h	Bit[7]: Gamma Offset Control1, 0: Auto offset1, 1:Manual offset1; Bit[6:0]: The manual written gamma offset.
3ah	***TSLB***	8	00h	Bit[7]: 0:Select even row, 1:Select odd row; Bit[6]:0:Select even column, 1:Select odd column; Bit[5]:Reserved ; If YUV422 is selected, the Sequence is: Bit[1:0]:Output YUV422 Sequence, 00: YUYV, 01: YVYU, 10: UYVY, 11: VYUY, If RGB565/RGB555/RGB444 is Selected, the Sequence is: Bit[4:0]: Output RGB565/RGB555/RGB444 Sequence, RGB565: 00h: R5G3H,G3LB5, 01h: B5G3H,G3LR5, 02h: B5R3H,R2LG6, 03h: R5B3H,B2LG6, 04h: G3HB5,R5G3L, 05h: G3LB5,R5G3H, 06h: G3HR5,B5G3L, 07h: G3LR5,B5G3H, 08h: G6B2H,B3LR5, 09h: G6R2H,R3LB5; RGB555: 0Ah: 0R5G2H,G3LB5, 0Bh: G3LB5,0R5G2H, 0Ch: R5G3H,G2LB50, 0Dh: G2LB50, R5G3H, 0Eh: B5G3H,G2L0,R5, 0Fh: R5G3H,G2L0,B5, 10h: B50G2H,G3LR5, 11h: R50G2H,G3LB5, RGB444: 12h: 4'b0R4,G4B4, 13h: G4B4,4'b0R4, 14h: 4'b0B4,G4R4, 15h: G4R4,4'b0B4, 16h: R4G4,B44'b0, 17h: B44'b0,R4G4, 18h: B4G4,R44'b0, 19h: R44'b0,B4G4,

				1Ah: B4G4,R4B4, 1Bh: R4G4,B4R4, 1Ch: R4G2H0,G2LB40, 1Dh: B4G2H0,G2LR40, 1Eh: B40G3H,G1L0R40, 1Fh: R40G3H,G1L0B40;
3bh	***De1Ctr***	8	eah	Bit[7]: New De-noise Control, 0: Disable de-noise, 1: Enable de-noise. Bit[6]: Select center pixel or median value for new denoise 0:Center pixel value 1: Median value Bit[5:4]:Threshold of grid correction for new denoise 00:1/32*SumM_Sum2 01:3/32*SumM_Sum2 10:1/8*SumM_Sum2 11:1/4*SumM_Sum2 Bit[3]: Select median value or G_offset_MD for old denoise 0: G_offset_MD 1: Median Bit[2]: Select SumM_Sum1 or SumM_Sum2 for old denoise 0: Select SumM_Sum1 or SumM_Sum2 1: Select SumM_Sum1 Bit[1]: Consider the threshold of grid correction or not(new) 0:Not consider 1: Consider Bit[0]: Grid correction for new denoise, 0:On, 1: Off.
3ch	***Y_COEF_K1***	8	40h	Y Coefficient for new Contrast
3dh	***COM8***	8	59h	Common Control D, Bit[7:4]: Total rows number(M3) for CK-GATE subsample; Bit[3:0]: Total columns number(N3) for CK-GATE subsample.
3eh	***TAREG2***	8	38h	Bit[7]: Digital LDO power down control: 0: LDO normal , 1: Power down LDO (When power down LDO,VDDD=1.45V,and low power) Bit[6:5]:LDO output control : 00:1.45V 01:1.5V 11:1.55V 11:1.65V Bit[4]: Clock DBR select: 0:Mclk_isp2, 1:1/2 mclk_isp2 Bit[3]: Power down DBR control: 0:DBR normal, 1:Powerdown DBR,(when power down Doubler,VDD3=VDD3A). Bit[2]:VDD3 control: 0:VDD3=3.4V, 1:VDD3=3.56V. Bit[1]: VDD3_PR_SEL: 0: VDD3_PR=VDD3, 1:VDD3_PR=VDD3A. Bit[0]: VDD3_TX_SEL: 0: VDD3_TX=VDD3, 1:VDD3_TX=VDD3A.
3fh	***OFF_MUX OFFSET_MO***	8	a0h	Bit[7]: Gamma Offset Control2, 0: Manual offset2, 1: Auto offset2; Bit[6:0]: The manual written gamma offset.
40h	***k0***	8	28h	Gamma Correction Slop Coefficients 0.
41h	***k1***	8	28h	Gamma Correction Slop Coefficients 1.
42h	***k2***	8	30h	Gamma Correction Slop Coefficients 2.
43h	***k3***	8	29h	Gamma Correction Slop Coefficients 3.
44h	***k4***	8	23h	Gamma Correction Slop Coefficients 4.
45h	***k5***	8	1bh	Gamma Correction Slop Coefficients 5.
46h	***k6***	8	17h	Gamma Correction Slop Coefficients 6.
47h	***k7***	8	0fh	Gamma Correction Slop Coefficients 7.
48h	***k8***	8	0ch	Gamma Correction Slop Coefficients 8.
49h	***k9***	8	0bh	Gamma Correction Slop Coefficients 9.
4ah	***SHR_DR_SEL VBLANK_CNTL DOUBLE_RESET_CNTL NULL_LN_RST_CNTL SUBSAMPLE***	8	18h	Bit[7]: 0: The signal SHR remain default we set during Dark-Row time, 1: The signal SHR is the same as SHS during Dark-Row time; Bit[6:5]: 00: The value of vblank is 4, 01: The value of vblank is {DM_LNH, DM_LNL[7:1]}+4, 1x: The value of vblank is {DM_LNH, DM_LNL[7:0]}+4; Bit[4]: 0: Normal reset, 1: Line reset 2 active lines (Double reset); Bit[3]: 0: Null line don't reset, 1: Null line (Line which don't read out) reset; Bit[2]:Row subsample enable: 0:Realize row subsample in sensor_control module, 1:Don't realize row subsample in sensor_control module. Bit[1]: Windowing Control, 0: Normal output (default value),

				1: Enable windowing. Bit[0]:1:Realize 1/2 col subsample, output 328colx488row ; 0:Normal output 648colx488row ;
4bh	***k10***	8	09h	Gamma Correction Slop Coefficients 10.
4ch	***k11***	8	08h	Gamma Correction Slop Coefficients 11.
4dh	***Y_COEF_K3***	8	40h	Y Coefficient for new Contrast
4eh	***k12***	8	07h	Gamma Correction Slop Coefficients 12.
4fh	***k13***	8	05h	Gamma Correction Slop Coefficients 13.
50h	***k14***	8	04h	Gamma Correction Slop Coefficients 14.
51h	***TARGET2/TARGET2D/TARGET2_F***	8	93h	Color Correction Coefficients 1.
52h	***TARGET3/TARGET3D/TARGET3_F***	8	04h	Color Correction Coefficients 2.
53h	***TARGET4/TARGET4D/TARGET4_F***	8	87h	Color Correction Coefficients 3.
54h	***TARGET6/TARGET6D/TARGET6_F***	8	88h	Color Correction Coefficients 4.
55h	***BRIGHT***	8	00h	Brightness control: Bit[7]: 0:Positive , 1:Negative Bit[6:0] : value
56h	***Y_COEF***	8	40h	When 0xb4[4] : 0: Y Coefficient for new Contrast. 1: Y Coefficient for old Contrast.
57h	***TARGET7/TARGET7D/TARGET7_F***	8	82h	Color Correction Coefficients 5.
58h	***TARGET8/TARGET8D/TARGET8_F***	8	8dh	Color Correction Coefficients 6.
59h	***Y_COEF_K4***	8	40h	Y Coefficient for new Contrast
5ah	***CC_COEF_SEL COLOR_DIS CHANGE_F PAGE_F COLOR_TEM_DIS ADJ_EN***	8	68h	Bit[7]: 0:Select the Color Correction Coefficients of indoor, 1:Select the Color Correction Coefficients of outdoor, Bit[6]: 1: Enable Color Correction Coefficients switch, 0: Disable Color Correction Coefficients switch . Bit[5]:The mode of f light 1: Select F-light Coefficients if the statistic number of F-light is more than COLOR_TEM_TH in FRM_CNT_TH 0: Select F-light Coefficients if COLOR_TEM is 1 Bit [4]: 0:Select the Color Correction Coefficients of non-F light, 1:Select the Color Correction Coefficients of F light. Bit[3]: 1:Use auto selected Coefficients (normal or outdoor or f-light) for color correction; 0:Don't use f-light Coefficients for color correction; Bit[2]: 0:Enable color correction denoise 1:Disable color correction denoise Bit[1:0] :Reserved
5bh	***FRINGE***	8	02h	Bit[7]: 0:do color correction for purple fringe, 1:do not do color correction for purple fringe. Bit[6]: 0:do saturation for purple fringe, 1:do not do saturation for purple fringe. Bit[5:4]: Color Correction to the reference purple fringe pixels disable control Bits 00: the one reference purple fringe pixels don't do color correction, 01: the three reference purple fringe pixels don't do color correction, 10: the five reference purple fringe pixels don't do color correction, 11: the six reference purple fringe pixels don't do color correction. Bit[3:0]:edge_step threshold for purple fringe pixel correction.
5ch	***SPEC_SEL GLB_GAIN_TH***	8	58h	Bit[7:6]: Posterize mode Selection, 00: 2 levels, 01: 3 levels, 10: 4 levels, 11: 5 levels. Bit[5:0]: GLB_GAIN_TH for CC adjust, GLB_GAIN>GLB_GAIN_TH,do adjust
5dh	***TXD_OFFSET_F / ANALOG_PDN_R***	8	42h	Bit[7:6]:Control the falling edge offset between TXD and PRST. Bit[5:0]:Control the rising edge of the signal (ANALOG_PDN)which is for analog Clock power down.
5eh	***TXD_OFFSET_R/PRST_R***	8	5eh	Bit[7:6]:Control the rising edge offset between TXD and PRST. Bit[5:0]:Control the rising edge of the signal (PRST) ;

5fh	***DARK_SEL,DARK_ SWITCH***	3	04h	Bit[7:0]:Reserved
60h	***Ma_Th_Ctr1***	8	e5h	Bit[7:4]: bright threshold for judge macula; Bit[3:0]: dark threshold for judge macula.
61h	***Ma_Th_Ctr2***	8	72h	Bit[7:0]: Reserved;
65h	***G_COEF***	8	46h	Lens shading correction gain for G pixel.
66h	***B_COEF***	8	46h	Lens shading correction gain for B pixel.
67h	***MANU***	8	80h	Manual U value (Effectively only when register DICOM [5] is high).
68h	***MANV***	8	80h	Manual V value (Effectively only when register DICOM [5] is high).
69h	***DICOM1***	8	00h	Dither Control 1, Bit[7]: YCBCR RANGE Selection, 0: Y/CB/CR: 0~255, 1: Y: 16~235, CB/CR: 16~240; Bit[6]: Negative Pixel, 0: Normal, 1: Enable negative pixel (When the pixel's Y_AVER is not smaller than 128); Bit[5]: Output UV Value Selection, 0: Output normal value, 1: Output fixed value set by registers MANU and MANV; Bit[4]: U、V Dither when in YCBCR Mode/B、R Dither when in RGB Mode, 0: Low 2 bits, 1: Low 3 bits; Bit[3]: Y Dither when in YCBCR Mode/G Dither when in RGB Mode: 0: Low 2 bits, 1: Low 3 bits; Bit[2]: Y dither enable/G dither enable; Bit[1]: U、V dither enable/B、R dither enable; Bit[0]: Negative Image Control, 0: Normal image, 1: Negative image.
6ah	***DE_GAIN_EN DE_GAIN_EN_CBR DE_GAIN_EN_AUT O SKIN_M_EN GNGAINREG***	8	81h	Bit[7]: Increase White Pixels, 0: Disable, 1: Enable; Bit[6]: Wipe off b_gain and r_gain of (b+r-2*g); Bit[5]: Used with bit[6], auto select wipe off gain or not; Bit[4]: SKIN_M_EN; Bit[3]:Reserved Bit[2:0]: G channel Gain (Bit2~Bit0 is used as Green Gain[5:3]).
6bh	***COM9***	8	02h	Common Control 9, Bit[7]: 0: Select column gate subsample for CK-GATE subsample, 1: Select HREF for CK-GATE subsample; Bit[6]:Reserved Bit[5:4]: Average Weight Selection; Bit[3] 0: Normal, 1: CKSUB is ahead one MCLK(YUV) or PCLK (Rawdata) of DATA; Bit[2] 0: normal, 1: CKSUB is ahead 0.5 MCLK(YUV) or PCLK (Rawdata) of DATA; Bit[1]: 0: No CK-GATE when HREF=0, 1: Always has CK-GATE; Bit[0]: 0: Disable CK-GATE subsample, 1: Enable CK-GATE subsample.
6ch				Bit[7:0]:Reserved
6dh	***INT_TIM_TH***	8	c0h	INT_TIM compare mark Bit[7]:1:don't need judge INT_TIM and Y_EVER's value for judge macula's edge; 0,need judge INT_TIM and Y_EVER's value for judge macula's edge Bit[6:0]:INT_TIM_LA_TH,INT_TIM threshold,if INT_TIM more than INT_TIM_LA_TH,and macula isn't occur.
6eh	***GLB_GAIN_TH***	6	20h	Global gain threshold.
6fh	***DICOM2***	8	7fh	Bit[7]: PRE_DATFOR Control, 0: Enable PRE_DATFOR, 1: Bypass PRE_DATFOR Bit[6:0]: Y threshold for dither, and dither is only enabled for the pixel: Y<2*DICOM2[6:0].
70h	***SwiCtr1***	8	0fh	Bit[7]:Stop_Sram--SRAM Control, 0: Enable SRAM, 1: Disable SRAM; Bit[6:4]: Special Effect Selection, 000: Normal RGB data, 011: Sketch,

				100: Cuprum relievo, 101: Blue relievo, 110: Black relievo, 111: White relievo, Default: Gray relievo. Bit[3]:Edge_Switch--Edge Enhancement Control, 0: Disable edge enhancement, 1: Enable edge enhancement; Bit[2]: De_Flat_En-consider Less_flat signal for denoise or not 0:Consider 1:Not consider Bit[1]:Bp_Switch-- Bad Pixel Correction Control, 0: Disable bad pixel correction, 1: Enable bad pixel correction; Bit[0]:Lpf_Switch--De-noise Control, 0: Disable de-noise, (3b= 7'h08 at the same time) 1: Enable de-noise.
71h	***SwiCtr2***	8	0ch	Bit[7]: Cross Talk Correction Control 1, 0: Disable cross talk correction in vertical direction, 1: Enable cross talk correction in vertical direction; Bit[6]: Cross Talk Correction Control 2, 0: Disable cross talk correction in horizontal direction, 1: Enable cross talk correction in horizontal direction; Bit[5]: Black Sun Correction of Last Frame Control, 0: Disable black sun correction of last frame, 1: Enable black sun correction of last frame; Bit[4]: Black Sun Correction Control, 0: Disable black sun correction , 1: Enable black sun correction ; Bit[3]: Grid Correction Control, 0: Disable grid correction, 1: Enable grid correction; Bit[2]: Cluster Correction Control, 0: Disable cluster correction, 1: Enable cluster correction; Bit[1]: Color Fringe Correction Control, 0: Disable color fringe correction, 1: Enable color fringe correction; Bit[0]: Auto De-noise in Low Light Control, 0: Disable auto de-noise in Low Light, 1: Enable auto de-noise in Low Light.
72h	***BpcCtr***	8	4ch	Bit[7:0]: Reserved
73h	***DenCtr1***	8	37h	Bit[7:4]: Base threshold for de-noise; Bit[3:0]: Default global gain threshold for de-noise.
74h	***DenCtr2***	8	6dh	Bit[7:0]: Reserved
75h	***DenCtr3***	8	8ah	Bit[7:0]: Reserved
76h	***DenCtr4***	8	88h	Bit[7:0]: Reserved
77h	***DenCtr5***	8	8ah	Bit[7:0]: Reserved
78h	***IntCtr***	8	ffh	Bit[7:0]: Reserved
79h	***EdgCtr1***	8	64h	Bit[7:4]: Based value for edge modification. Bit[3]:Edg_Off_Step--he Speed of Edge Compensation According to Gain Difference, 0: 1/4 1: 1/8; Bit[2:1]:Edg_En_Max--Add or Minus Maximum Value on Edge, 00: 1/4*Y_CEN 01: 1/2*Y_CEN; 10: 3/4*Y_CEN 11: Y_CEN; Bit[0]:Edg_Off_Mode--Edge Compensation Mode Selection, 0: Auto, 1: Manual.
7ah	***EdgCtr2***	8	23h	Bit[7:4]: Positive Edge Enhancement Gain, 0000:0.125, 0001:0.50, 0010:1.00, 0011:1.50, 0100:1.75, 0101:2.25, 0110:2.50, 0111:3.00, 1000:3.25, 1001:3.75, 1010:4.00, 1011:4.50, 1100:4.75, 1101:5.50, 1110:5.75, 1111:8.00. Bit[3:0]: Negative Edge Enhancement Gain, 0000:0.125, 0001:0.50, 0010:1.00, 0011:1.50,

				0100:1.75, 0101:2.25, 0110:2.50, 0111:3.00, 1000:3.25, 1001:3.75, 1010:4.00, 1011:4.50, 1100:4.75, 1101:5.50, 1110:5.75, 1111:8.00.
7bh	***EdgCtr3***	8	58h	Bit[7:4]: The reduced value for color fringe correction (*4); Bit[3]: Thin Edge Control, 0: Disable thin edge, 1: Enable thin edge; Bit[2:0]: The minimal value of sobel (*2).
7ch	***SobMax***	8	55h	Bit[7]: Reserved; Bit[6:4]: Threshold for sobel difference (2^Bit[6:4]); Bit[3]: Reserved; Bit[2:0]: Threshold for sobel difference (2^Bit[2:0]).
7dh	***ColCtr***	8	RO/50h	Bit[7:4]: The restricted threshold for color fringe correction - Blue Threshold (*4); Bit[3]: Color Fringe Correction Mode Selection for Color Correction, 0: Only blue (B>G) edge, 1: All edge; Bit[1]:Ed_Step--Choose the Value of Edge Maximum, 0: 128, 1: 64; Bit[0]:Gray_judge--Gray Region Edge Judgement Control, 0: Disable, 1: Enable;
7eh	***MacCtr1***	8	24h	Bit[7:4]:TH_add--Control the diameter of the black sun (*4); Bit[3:0]:Mac_Time--Maximal INT_TIM to enable black sun correction (*16).
7fh	***MacCtr2***	8	3ch	Bit[7]:Mac_auto_manu --Black Sun Correction Control, 0: Auto, 1: Manual; bit[6]:Max_Clc--Clear the Mean Value of Black Sun Correction at the End of the Frame, 0: Off, 1: On; bit[5:0]:Mac_Th--he Modified Threshold for Black Sun Correction (*4).
80h	***AE_MODE***	8	92h	Bit[7]: AE test mode conteol 1 :normal 0 :test mode Bit[6]: 0 : AE adjusts every two frames ; 1: AE adjusts every frame enable Bit[5:4]:G_MIN_SLOPE When INT_TIM >INT_MID ,gain Coefficients: 00: 0 ; 01: 1 ; 10: 2 ; 11: 3 . Bit[3:2]: P_OE_SEL (what is P_OE_SEL) 00:/2^15 01:/2^16 10:/2^17 11:/2^18 Bit[1]: 0:Choose 60HZ step ,1:Choose 50HZ step. Bit[0]: AE is adjusted by men, effective when test mode(0x80[7]==1'b0)
81h	***AE_SPEED***	8	00h	Bit[7:4] : The speed of adjusting from light to dark Bit[3:0] : The speed of adjusting from dark to light
82h	***GLB_MIN1***	8	1bh	Global Gain Minimum 1.
83h	***GLB_MAX1***	8	37h	Global Gain Maximum 1.
84h	***GLB_MIN2***	8	39h	Global Gain Minimum 2.
85h	***GLB_MAX2***	8	5dh	Global Gain Maximum 2.
86h	***GLB_MAX3***	8	77h	Global Gain Maximum 3.
87h	***GLB_GAIN***	8	16h	Global Gain for sensor.
88h	***Y_AVER***	8	RO	Y_AVER value. **Read Only.**
89h	***INT_MAX_MID***	8	7d	Bit[7:3]:INT_MAX, Bit[2:0]:INT_MID.
8ah	***INT_STEP_50***	8	99h	50HZ Banding Filter Value low 8 bits, the high 1 bit at register 0x13[4] (COM8[4]).
8bh	***INT_STEP_60***	8	7fh	60HZ Banding Filter Value low 8 bits, the high 1 bit at register 0x13[5] (COM8[5]).
8ch	***INT_TIM[15:8]***	8	01h	Integration time MSB; Integration time LSB.
8dh	***INT_TIM[7:0]***	8	cbh	
8eh	***Y_OV_TH***	8	2c h	When Y_AVER>240+Y_OV_TH[3 :0]|| Y_AVER <Y_OV_TH[7 :4],if AE adjusts every frame enabled, it will adjusts every frame.
8fh	***INT_MIN***	8	82h	Bit[7]: 0: The minimum integration time is banding filter value, 1: The minimum integration time is set in the register INT_MIN [6:0].
90h	***OFFSET_CTR1,INT_***	8	a0h	Bit[7]: OFFSET_CTR1:

	TIM_TH			1: 1/2 will be used for auto offset adjustment, 0: 1/4 or 5/8 will be used for auto offset adjustment; Bit[6:0]: Integration time threshold for auto offset adjustment in high light scene.
91h	***OFFSET_CTR2,Y_AVER_TH***	8	e0h	Bit[7]: OFFSET_CTR2; 1: When OFFSET_CTR1 is set to 1'b0, 1/4 will be used for auto offset adjustment, 0: When OFFSET_CTR1 is set to 1'b0, 5/8 will be used for auto offset adjustment; Bit[6:0]: Y_AVER threshold for auto offset adjustment in low light scene.
92h	***DM_LNL***	8	09h	Dummy line inserted after active line low 8 Bits
93h	***DM_LNH***	8	00h	Dummy line inserted after active line high 8 Bits
94h	***TAR_BASE0***	8	02h	Bit[7:4]: The threshold for overexposure pixel judgment; Bit[3:0]: Control the start of AE.
95h	***TAR_BASE1***	8	88h	Bit[7:4]: Parameter1 for Y_AVER modifying; Bit[3:0]: The smallest value the target brightness can achieve.
96h	***YBRIGHT_TH***	8	b5h	Bit[7:4] : The speed of AE adjustment from dark to bright; Bit[3:0] : Threshold2 for outdoor scene judgment.
97h	***AE_TAR2***	8	3Ch	Bit[7]: Reserved Bit[6 :0] :Y target value1 for F light.
98h	***COM1***	8	8ah	Bit[7]: Data for AE Selection 0: Choose YUV data to do AE, 1: Choose Raw Data to do AE. Bit[6]: Minimum Step Control 1: 2 steps, 0: 1 step. Bit[5:4]: Exposure Center Window Selection 00: ROW*12/16, COLUMN*12/16, 01: ROW*10/16, COLUMN*10/16, 10: ROW* 8/16, COLUMN* 8/16, 11: ROW* 6/16, COLUMN* 6/16. Bit[3]: The Speed of Digital Gain Adjustment 0 : Slow, 1 : Fast. Bit[2:0]: WEIGHT_SEL 000: 4/8*center+4/8*border, 001: 5/8*center+3/8*border, 010: 6/8*center+2/8*border, 011: 7/8*center+1/8*border, 100~111: center 100%.
99h	***DIG_GAIN_I2C***	8	10h	The value of DIG_GAIN
9ah	***INT_TIME_TH***	8	50h	Threshold1 for outdoor scene judgment.
9bh	***y0l_g***	8	f4h	The vertical center low 8 bits of G (Vertical center).
9ch	***xol_g***	8	44h	The horizontal center low 8 bits of G (Horizontal center).
9dh	***GLB_GAIN_I2C***	8	1bh	Global gain.
9eh	***EffCtr***	8	c4h	Bit[7]: Thin edge judgment Control(new) 0:Disable 1: Enable Bit[6]: Thin edge enhancement Control(new) 0:Disable 1: Enable Bit[5]: Auto select old/new denoise according to SKY_SCENE signal Control 0: Disable(decide by De1Ctr[7]) 1:Enable(indoor select old denoise; outdoor decide by De1Ctr[7]) Bit[3:0]: Threshold for thin edge judgment(*2);
9fh	***DIG_GAIN_MAX***	8	64h	Bit[7:4]: It is set to limit the speed of AE to avoid over adjusting.the bigger it is ,the quicker the AE adjusting. Bit[3:0]: DIG_GAIN_MAX[3:0]*16 as the limit of DIG_GAIN
a0h	***AWB_CTR_SET***	8	00h	Bit[7:2]: Reserved; Bit[1:0]: Used to control R, G1, B or G2 average value (used with the register RGB_AVER(0xaf),)1 00: R_aver, 01: G1_aver, 10: B_aver, 11: G2_aver.
a1h	***AWB_TH1_SET***	8	31h	Bit[7:4]: Auto white balance lock boundary; Bit[3:0]: Auto White Balance update speed.
a2h	***BLU_GAIN_TH1***	8	0bh	Bit[7:6]: Reserved; Bit[5:0]: Minimum blue gain for indoor scene.
a3h	***BLU_GAIN_TH2***	8	20h	Bit[7:6]: Reserved;

				Bit[5:0]: Maximum blue gain for indoor scene.
a4h	***RED_GAIN_TH1***	8	09h	Bit[7:6]: Reserved; Bit[5:0]: Minimum red gain for indoor scene.
a5h	***RED_GAIN_TH2***	8	26h	Bit[7:6]: Reserved; Bit[5:0]: Maximum red gain for indoor scene.
a6h	***COUNT_EN***	8	04h	White pixels count threshold.
a7h	***BASE_B_GAIN***	8	19h	Bit[7:5]:Reserved; Bit[4:0]: Base B gain.
a8h	***BASE_R_GAIN***	8	15h	Bit[7:5]:Reserved; Bit[4:0]: Base R gain.
a9h	***AWB_GB_LIM***	8	12h	Bit[7:6]: Reserved; Bit[5:0]:AWB criterion: B.
aah	***AWB_GR_LIM***	8	12h	Bit[7:6]:Reserved; Bit[5:0]:AWB criterion: R.
abh	***AWB_BR_LIM***	8	16h	AWB criterion: BR.
ach	***AWB_G_LOW***	8	3ch	AWB criterion: G_LOW.
adh	***AWB_G_HIG***	8	f0h	AWB criterion: G_HIGH.
aeh	***F_LIGHT_TH***	8	57h	Bit[7:4]: B limit to estimate F light; Bit[3:0]: R limit to estimate F light.
afh	***RGB_AVER***	8	RO	Read out R/G/B average value, used with the register AWB_CTR_SET[1:0](0xa0[1:0]).
b0h	***SAT_CTR1***	8	20h	Bit[7] :Page select for register 0xB1/0xB2/0xB4 , 0: NF light 1:F light Bit[6:0] SAT_CTR1[6:0] is used as Y pixel threshold for auto saturation(for dark region).
b1h	***CB_COEF***	8	c6h/f0h	Cb Coefficient low 8 bit for Color Saturation
b2h	***CR_COEF***	8	cch/a0h	Cr Coefficient low 8 bit for Color Saturation
b3h	***SAT_CTR2***	8	4fh	Bit[7:4]: used as Yavaer threshold for auto saturation. Bit[3:0]:Used to select the mean of the gray section for test
b4h	***SAT_CTR3_NF/SAT_CTR3_F***	8	e1h	Write 0xb0[7] to select adjust NF or F light Bit[7]: 0: Off sat mode for dark region 1: On sat mode for dark region Bit[6]:Gray section denoise mean select Bit[5]:Gray section denoise switch Bit[4]: New contrast switch 0:New contrast 1:Old contrast Bit[3]: High bit of Cb coefficient. Bit[2]: High bit of Cr coefficient. Bit[1]: Reserved. Bit[0]: 0: Only use !F-light Coefficients for Saturation; 1: Use auto selected Coefficients for Saturation: (when F-light is determinated, use F-light Coefficients, else use !F-light Coefficients)
b6h	***MAN_R***	8	80h	Define R value.
b7h	***MAN_G***	8	80h	Define G value.
b8h	***MAN_B***	8	80h	Define B value.
b9h	***TEST_MODE***	8	00h	8'h00: normal output; 8'h01~8'h0f: overlay vertical bar pattern; 8'h10~8'h1f: overlay horizontal bar pattern; 8'h20~8'h2f: overlay vertical gradual pattern; 8'h30~8'h3f: overlay horizontal gradual pattern; 8'h40~8'h5f: overlay manual pattern; 8'h60~8'h7f: overlay auto scan mode; 8'h80~8'h8f: fixed vertical bar pattern; 8'h90~8'h9f: fixed horizontal bar pattern; 8'ha0~8'haf: fixed vertical gradual pattern; 8'hb0~8'hbf: fixed horizontal gradual pattern; 8'hc0~8'hdf: fixed manual pattern; 8'he0~8'hff: fixed auto scan mode.
bah	***AVER_GB_LIM*** ***AVER_GR_LIM***	8	44h	Bit7:4]: The threshold of B_AVER-G_AVER to judge wipe off gain or not. If B_AVER-G_AVER>AVER_GB_LIM, don't wipe off gain (Used with 0xa0[5]); Bit3:0]: The threshold of R_AVER-G_AVER，The same as AVER_GB_LIM.
bbh	***BANK***	8	03H	Bit[7:2]:Reserve Bit[1]:Odd-column average control 1:Average disable 0:Average enable Bit[0]:Even-column average control

				1:Average disable 0:Average enable
bch	***y0h_r VFLIP_MUX HFLIP_MUX x0h_r***	8	0dh	Bit[7:5]: Reserved; Bit[4]: The vertical center high 1 bit of R; Bit[3]: VFLIP_MUX, when VFLIP, it is for test when set to 1'b1; Bit[2]: HFLIP_MUX, when HFLIP, it is for test when set to 1'b1; Bit[1:0]: The horizontal center high 2 bits of R.
bdh	***y0l_r***	8	F4h	The vertical center low 8 bits of R (Vertical center).
beh	***x0l_r***	8	44h	The horizontal center low 8 bits of R (Horizontal center).
bfh	***SHR_R***	7	26h	Control the rising edge of the signal (SHR)
c0h	***SHR_F***	8	34h	Control the falling edge of the signal (SHR)
c1h	***TX_F***	7	47h	Control the falling edge of the signal (TX)
c2h	***SHS_F***	7	58h	Control the falling edge of the signal (SHS)
c3h	***READEN_F***	8	90h	Control the falling edge of the signal (READEN)
c4h	***SHR_TX_R_OFFSET***	8	33h	Bit[7:4]:Control the offset between the falling edge of TX and the rising edge of SHS; Bit[3:0]:Control the offset between the falling edge of SHR and the rising edge of TX ;
c5h	***B_STEP_LIMIT R_STEP_LIMIT***	8	aah	Bit[7:4]: B Step Limit, When b_differ (B_aver ± offerset - G_aver) is larger than the limit, use step 2, else 1; Bit[3:0]: R step limit (The same to B).
c6h	***B_R_PURE***	8	aah	Pure B or Pure R Threshold, Bit[7:4]: Pure B threshold; Bit[3:0]: Pure R threshold.
c7h	***COUNT_SEL OUTDOOR_EN PURE_EN OUT_STATE B_pure R_pure***	8	28	Bit[7:5]:Set as white pixels count threshold like reg 2ah(the proportion of view image) 000:1/32 001:1/16 010:3/128 011:1/64 Others:counter_en(0xA6); Bit[4]:Outdoor_en ,outdoor model control; Bit[3]:Open pure function: 0:Disable 1:Enable; Bit[2]:Out_state(outdoor symbol from AE,read only); Bit[1]: Pure b ,read only; Bit[0] :Pure r ,read only.
c8h	***BLUE_GAIN_LOW_OUT***	6	0dh	Bit[7:6]: Reserved; Bit[5:0]: Minimum blue gain for outdoor scene.
c9h	***BLUE_GAIN_HIG_OUT***	6	10h	Bit[7:6]: Reserved; Bit[5:0]: Maximum blue gain for outdoor scene.
cah	***PRST21_R***	8	5ah	Control the rising edge of the signal (PRST21)
cbh	***TX21_F1***	8	61h	Control the first falling edge of the signal (TX21)
cch	***TX21_F2***	8	69h	Control the second falling edge of the signal (TX21)
cdh	***PRST22R***	8	6bh	Control the rising edge of the signal (PRST22)
ceh	***TX22_F1***	8	72h	Control the first falling edge of the signal (TX22)
cfh	***TX22_F2***	8	7ah	Control the second falling edge of the signal (TX22)
d0h	***F_OFFSET***	8	00h	The Offset of F light, Bit[7:4]: B offset, MSB is sign bit; Bit[3:0]: R offset, MSB is sign bit.
d1h	***NF_OFFSET***	8	00h	The Offset of non-F light, Bit[7:4]: B offset, MSB is sign bit, Bit[3:0]: R offset, MSB is sign bit.
d2h	***IS_A_LIGHT DARK_ROW_OEEN GAIN_DIFF***	8	58h	Bit[7]: A light state, read only; Bit[6]: Dark row oeen, decide the color gain in darkrow; Bit[5]: Reserved; Bit[4:0]: Gain_diff (Used to wipe off gain function).
d3h	***RED_GAIN_LOW_OUT***	6	09h	Bit[7:6]: Reserved; Bit[5:0]: Minimum red gain for outdoor scene.
d4h	***RED_GAIN_HIG_OUT***	6	24h	Bit[7:6]: Reserved; Bit[5:0]: Maximum red gain for outdoor scene.
d5h	***AVEREB_DIF_I2C***	5	00h	Bit[7:0]: Reserved
d6h	***AVEROG_DIF_I2C***	5	00h	Bit[7:0]: Reserved
d7h	***AVEREG_DIF_I2C***	5	00h	Bit[7:0]: Reserved
d8h	***AVEROR_DIF_I2C***	5	00h	Bit[7:0]: Reserved
d9h	***PRST_F1***	8	24h	Control the falling edge of PRST
dah	***H_START_H***	8	00h	When register 0x4a[1] is high, analog windowing is enabled, X_WIN_START high 8 bits (low 2 bits at VH_ADD_L[1:0]).

dbh	***H_END_H***	8	a2h	When register 0x4a[1] is high, analog windowing is enabled, X_WIN_END high 8 bits (low 2 bits at VH_ADD_L[3:2]).
dch	***V_START_H***	7	00h	When register 0x4a[1] is high, analog windowing is enabled, Y_WIN_START high 8 bits (low 2 bits at VH_ADD_L[5:4]).
ddh	***V_END_H***	7	7ah	When register 0x4a[1] is high, analog windowing is enabled, Y_WIN_ END high 8 bits (low 2 bits at VH_ADD_L[7:6]).
deh	***VH_ADD_L***	8	00h	When register 0x4a[1] is high, analog windowing is enabled, Bit[7:6]: Y_WIN_END low 2 bits, Bit[5:4]: Y_WIN_START low 2 bits, Bit[3:2]: X_WIN_END low 2 bits, Bit[1:0]: X_WIN_START low 2 bits.
dfh	***PRST_F2***	8	2ah	Control the falling edge of PRST for avoid black sun
e0h	***H_HSYNC_EDGE***	8	00h	Bit[7:4]:HSYNC rising edge[11:8]; Bit[3:0]:HSYNC falling edge[11:8];
e1h	***READEN_CNTL*** ***READEN_R***	6	02h	Bit[7:6]:Reserved Bit[5]: 0:Default,READEN pulse appear every line counter time; 1:READEN always is 1 . Bit[4:0]: Control the rising edge of READEN_R
e2h	***ISP_CK_CNTL*** ***HREF_CNTL***	8	0dh	Bit[7]:0:Default,ISP_CK_PDN signal is always 0; 1:ISP_CK_PDN pulse is being created every line; Bit[6]:0:Default,ANALOG_PDN signal is always 0; 1:ANALOG_PDN pulse is being created every line; Bit[5:4]:Control the PR_TX or DOUBLE_PR_TX pulse: 00:Every line have two reset pulse, 01,All line have a long reset pulse, 1x,Aall line have a short reset pulse. Bit[3]:1:Default,TX2 divide into 2 pulse, 0:The two pulse come to one. Bit[2:0]:Control the delay of HSYNCE to HREF_DAT 000:Delay four pclk; 001:Delay five pclk; 010:Delay six pclk; 011:Delay seven pclk; 100:Delay eight pclk; 101:Delay nine pclk; 110:Delay ten pclk. 111: Delay eleven pclk.
e3h	***DM_ROWL***	8	09h	Dummy line insert before active line low 8 Bits.
e4h	***DM_ROWH***	8	00h	Dummy line insert before active line high 8 Bits.
e5h	***ISP_CK_PDN_F***	8	92h	Control the falling edge of the signal (ISP_CK_PDN) which is for ISP Clock power down.
e6h	***ANALOG_PDN_F***	8	58h	Control the falling edge of the signal (ANALOG_PDN) which is for Analog Clock power down.
e7h	***ISP_CK_PDN_R***	6	14h	Control the rising edge of the ISP_CK_PDN .
e8h	***GAIN_BEG_0D***	8	11h	Curve line :the first beginning point
e9h	***GAIN_END_0D***	8	21h	Curve line :the first ending point
eah	***GAIN_BEG_1D***	8	22h	Curve line :the second beginning point
ebh	***GAIN_END_1D***	8	42h	Curve line :the second ending point
ech	***GAIN_BEG_2D***	8	43h	Curve line :the third beginning point
edh	***GAIN_END_2D***	8	83h	Curve line :the third ending point
eeh	***P_TH***	8	4ch	Probability threshold
efh	***SKIN_CTR***	4	0bh	Bit[7]: 0: Disable A light signing function, 1: Enable A light signing function; Bit[6]: 0: Disable white pixels signing function, 1: Enable white pixels signing function; Bit[5:4]: Reserved; Bit[3]: 0: Disable skin function, 1: Enable skin function; Bit[2]: 0: Disable hue rotate, 1: Enable hue rotate; Bit[1:0]: 0x: Display full resolution and can do hue with full resolution, 10: Only display skin area and only can do hue with skin area, 11: Display full resolution but only can do hue with skin area.
f0h	***GAIN_BEG_3D***	8	84h	Curve line :the forth beginning point
f1h	***BYPASS0***	8	00h	Bit[0]:Lens Correction, 0: Enable, 1: Disable Bit[1]:Gamma Correction, 0: Enable, 1: Disable Bit[2]:Color Intrpolation, 0: Enable, 1: Disable

				Bit[3]:Color Correction, 0: Enable, 1: Disable Bit[4]:CC_SP, 0: Enable, 1: Disable Bit[5]:Saturation, 0: Enable, 1: Disable Bit[6]:Contrast, 0: Enable, 1: Disable Bit[7]:Reserved
f2h	***SPEC_SWITCH FRM_CNT_TH***	8	0eh	Bit[7]: 1: Enable color separation control 0:Disable color separation control Bit[6:0:]select F-light Coefficients if the statistic number of F-light is more than COLOR_TEM_TH in FRM_CNT_TH
f6h	***GAIN_END_3D***	8	ffh	Curve line :the forth ending point
f7h	***Macula_TH***	8	8ah	set the integral time threshod whether to wipe off macula. Bit[7]: 0: Bit[6:0] the number of integral lines. 1: Bit[6:0] the number of integral steps.
f8h	***HUE_COS***	8	7fh	hue cosine cofficient range -1~0.99(0X80~0X7F) MSB is symbol
f9h	***HUE_SIN***	8	00h	hue sine cofficient range -1~0.99(0X80~0X7F) MSB is symbol
fbh	***COLOR_TEM_TH***	8	07h	select F-light Coefficients if the statistic number of F-light is more than COLOR_TEM_TH in FRM_CNT_TH
fch	***PID_BME***	8	3ah,RO	Product ID MSB
fdh	***VER_BME***	8	03h,RO	Product ID LSB

Table 5. BF3A03 all registers

8. Package Specifications

8.1 BF3A03A CSP Package Top View（unit：um）

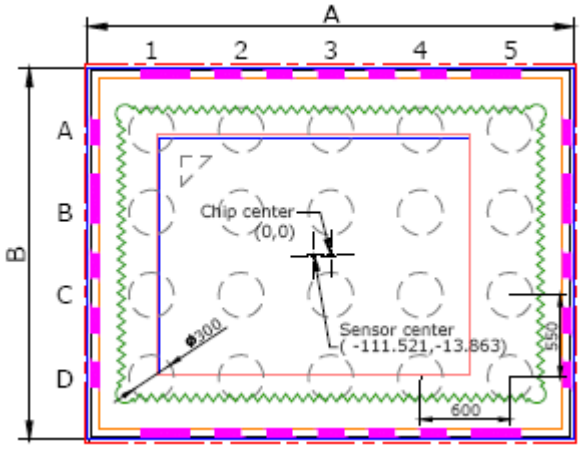


Figure 8. Package Top View

8.2 Ball Matrix Table

	1	2	3	4	5
A	VDD3A	RESET	D7	D5	VCLK
B	VSSA	PWDN	D6	D4	VSSD
C	SDA	VSYNC	D0	D1	D3
D	SCL	HREF	XCLK	D2	VDDIO

Table 6. Ball Matrix Table

8.3 BF3A03 Chip Pin Description

Pin Number	Name	Pin Type	Function/Description
A1	**VDD3A**	Power	Analog power supply.
A2	**RESET**	Input(1)*	Reset all registers to their default values. 0: Reset mode 1: Normal mode
A3	**D7**	Output	YUV/RGB image data output port [7].
A4	**D5**	Output	YUV/RGB image data output port [5].
A5	**VCLK**	Output	Pixel clock output.
B1	**VSSA**	Power	Analog ground.
B2	**PDN**	Input(0)**	Power Down Mode Selection. 0: Normal mode. 1: Power down mode.
B3	**D6**	Output	YUV/RGB image data output port [6].
B4	**D4**	Output	YUV/RGB image data output port [4].
B5	**VSSD**	Power	Digital ground.
C1	**SDA**	I/O	SCCB serial interface data I/O.
C2	**VSYNC**	Output	Vertical sync output.
C3	**D0**	Output	YUV/RGB image data output port [0].
C4	**D1**	Output	YUV/RGB image data output port [1].
C5	**D3**	Output	YUV/RGB image data output port [3].
D1	**SCL**	Input	SCCB serial interface clock input.
D2	**HREF**	Output	HREF(HSYNC) output.
D3	**XCLK**	Input	System clock input.
D4	**D2**	Output	YUV/RGB image data output port [2].
D5	**VDDIO**	Power	Power supply for I/O.

Table 7. Pin Description

Note:

** Input(1) represents an internal pull-up resistor.

** Input(0) represents an internal pull-down resistor.

8.4 CSP Package Mechanical Drawing (unit:um)

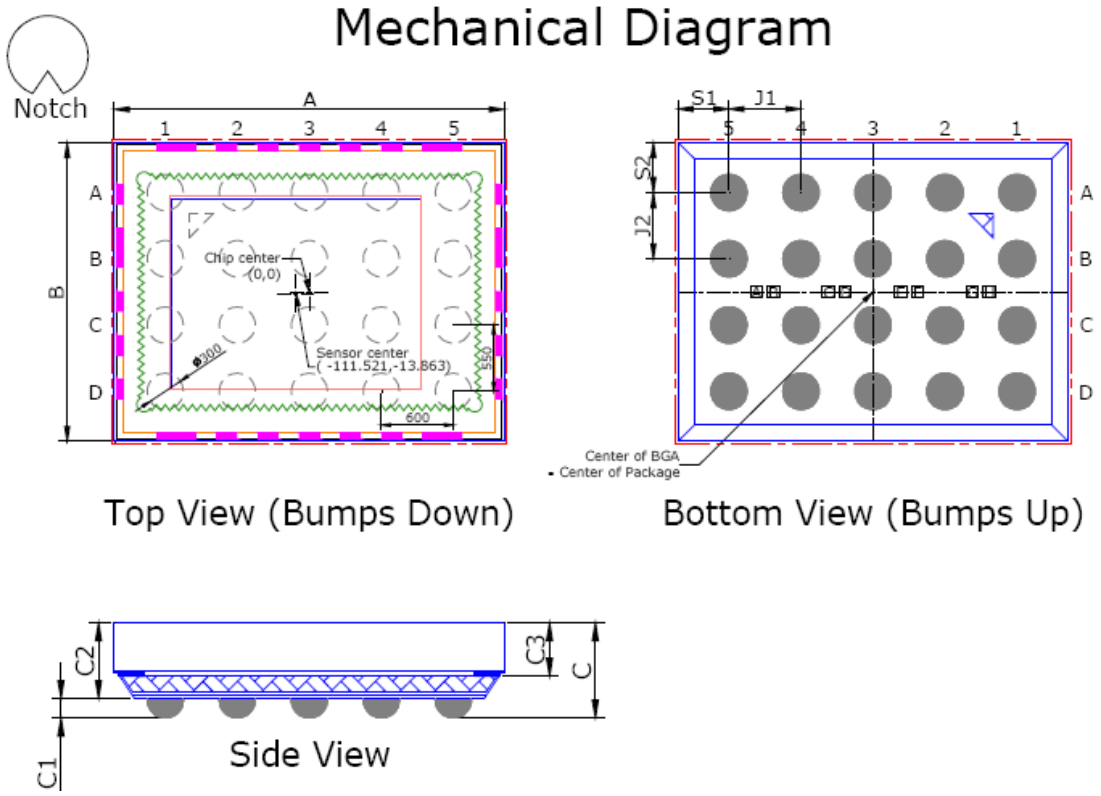


Figure 9. CSP Mechanical Drawing

8.5 CSP Dimensions

	Symbol	Nominal	Min	Max
		Unit（μm）		
Package Body Dimension X	**A**	3246	3221	3271
Package Body Dimension Y	**B**	2480	2455	2505
Package Height	**C**	790	730	850
Ball Height	**C1**	160	130	190
Package Body Thickness	**C2**	630	585	675
Thickness from top glass surface to wafer	**C3**	445	425	465
Ball Diameter	**D**	300	270	330
Total Ball Count	**N**	20		
Ball Count X axis	**N1**	5		
Ball Count Y axis	**N2**	4		
Pins Pitch X axis	**J1**	600		
Pins Pitch Y axis	**J2**	550		
Edge to Pin Center Distance along X	**S1**	423	393	453
Edge to Pin Center Distance along Y	**S2**	415	385	445

Table 8. CSP Dimensions

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- The information contained herein is subject to change without notice.

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